ABSTRACT OF THE DISCLOSURE

A data processor having: a peripheral circuit for selecting one of input terminals such as input channels, processing input data from the selected input terminal, requesting the transfer of the processing result, and outputting identification information (CH2 to CH0) which permits the identification of the selected input terminal; and a data transfer control circuit comprising a destination address register (DAR) with its low-order bits variable according to the identification information from the peripheral circuit, whereby the low-order bits of destinations can be controlled by the peripheral circuit in the transfer control circuit. The peripheral circuit is not required to comprise data registers for storing an input data processing result for each input terminal in one-to-one correspondence with the input terminals.